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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/858,308	05/15/2001	Zahid Najam	10736/9	3090

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EXAMINER	
COLEMAN, ERIC	
ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 01/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/858,308	NAJAM ET AL.	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 1-23 are rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for the invention where the reading and writing to/from memory, coprocessor and processor are dependent, does not reasonably provide enablement for independent reading and writing of data to/from memory, coprocessor and processor. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the invention commensurate in scope with these claims. The independent claims 1 and 11 claim independent read and writes independent of the coprocessor. However the disclosed invention utilizes a control logic for snooping whether the processor and coprocessor are to read or write to from memory for transfer therebetween. The memory is not unlimited size and therefore if the processor or coprocessor stores data too fast it would fill the memory and have to wait until to other (processor or coprocessor) read from the memory before continuing and therefore this operation is not independent (e.g., see pages 33 and 34 of the specification in the instant application).

Claim Rejections - 35 USC § 103

3. Claims 1-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gallotta (Patent No. 6,392,654)in view of Kowalczyk (patent No. 4,744,078).

4. Gallotta taught (as per claims 1,11,34) the invention substantially as claimed including a a data processing ("DP") system comprising:

a) a processor (18) (e.g., see fig. 1);

b) A co-processor (30,34)(e.g., see fig. 1);

c) An interface coupled with the processor (18) and said co-processor(30,34), said memory (first buffer 26) having at least two read/write ports for reading and writing data to said memory wherein said processor is coupled with one of said at least two ports and said co-processor is coupled with the other at least two ports (e.g., see figs. 1,2 and col. 4, lines 18-49)

d) control logic coupled with said at least two read/write ports [logic at least comprises the use of system elements with in the processors and coprocessor by drivers such as driver 32 for control of read/write to first buffer 26)(e.g., see col. 3, lines 23-59);

e) wherein said processor stores data intended for said co-processor to said memory and reads data stored by said co-processor from said memory (e.g., see col. 4, lines 18-49);

f) said coprocessor stores data intended for said processor to said memory and reads data stored by said co-processor from said memory independent of said co-processor said co-processor stores data intended for said processor to said memory and reads data stored from said memory independent of said processor (e.g., see col.

4, lines 18-49); and said control logic operative to facilitate the reading of said stored data by said processor and said co-processor; and wherein said processor and said coprocessor are capable of storing data to said memory substantially simultaneously.

5. Gallotta did not expressly detail (claims 1,11,34) that the storing of data to/from the memory by the processor was independent of said co-processor. However as the claims are understood, the independency pertains to a control logic that performs the control of read and write and determines when a read and write should occur and where the processor and coprocessor do not directly determine the status of the other for performing storing into the memory. Kowalczyk taught system that with a control logic (28) e.g., see figs 1 and 2) that controls storing of data to/from a dual port memory that does not require the connected processors to directly determine the status of other processors for storing data into the dual port memory (e.g., see col. 2, line 57-col. 4, line 31). The control of transfer via the multiple port memories in Gallotta and Kowalczyk provided for substantially simultaneous transfer of data therebetween.

6. It would have been obvious to one of ordinary skill to combine the teachings of Gallotta and Kowalczyk. Both references were directed toward control of transfer of data between system devices via a memory with plural input and outputs. Gallota taught the devices to transferring the data were processor and coprocessor that were on different cards or boards. In at least one implementation the transfer of data between the processor ,memory and coprocessor would have comprises transfer via a system bus. Kowalczyk taught the transfer was between a system bus and a network bus. Clearly the devices in a processing system storing data into a memory for transfer to another

device on another bus would have comprised processors. The addition of the control of transfer to be between system bus and network bus would have allowed the combined system to transfer data between processors in a system to co-processors that were connected in a network. This control would have relieved the processor from having to determine when the coprocessor was ready for transfer of data.

7. As to the limitations of claim 2,12,23,26 Gallotta taught the processors on different cards or boards and therefore the boundary would have comprised a printed circuit board to printed circuit board connected couple to the processor and co-processor (e.g., see figs 1, 2). The use of connectors that isolate the connected devices from the bus were well known in the art at the claimed invention. One of ordinary skill implementing the Gallotta and Kowalczyk system would have been motivated to use these tristate type connectors to at least protect the connected devices for electrical surges when not actively transferring data and to reduce power drain a from plural elements and connected to the bus and ensure stability of signals transferred bus without interference.

8. As per claim 3,4,13,14,27,35 Kowalczyk taught transfer between a system bus and a network bus. Therefore one of ordinary skill have been motivate to connect the best available network devices to the network bus. Since at least some network devices would have comprised different characteristics for the transferred data such as word length or encoding etc.(especially when they were from different manufacturers) then in at least one implementation of the Gallota and Kowalczyk teachings the boundary would

have comprised different protocols. Clearly the processor connected to the network bus would have comprised an network processor (e.g., see col. 2, lines 41-56).

9. As to claim 5,15,28,36 Gallotta taught the co-processor comprising a task specific processor (e.g., see col. 3, lines 23-65).

10. As per claim 6,7,16,17,29,30,37,38 One of ordinary skill would have been motivated to connected off the shelf components to aid the processor in processing data. Since the Kowakczyk taught a network bus one of ordinary skill would have been motivated to connected the system to various type of networks including the INTERNET. In applications that would be characteristic of searching volumes of data via the INTERNET one of ordinary skill would have been motivated to coupled a classification coprocessor and an content addressable memory to search for data especially when the co-processor is used a conventional search engine.

11. As per claims 8,9,18,19,31,39 Kowalczyk taught control logic signals via the connected buses when data is stored in the data memory (e.g., see col. 4, lines 1-31). Considering the devices connect to the buses would have comprised processor and co-processors (especially considering the teachings of Gallota) the signals to the bus would have been transmitted to the processor and co-processor.

12. As per claim 10,20,32,,40 Kowalczyk taught the memory comprises a dual ported synchronizing random access memory (10) e.g., see col. 2 lines 41-57). Since Kowalczyk did not detail refresh of the memory it would have been obvious to one of ordinary skill that the memory would have comprised a static random access memory. As to the burst capability of the memory since the memory is allowing switching of

transfer between two buses one of ordinary skill would have been motivated to select an off the shelf memory with burst capability to facilitate quick transfer when a lot of data was being transferred.

13. As per claims 21,22,33,41 The control logic of Kowalczyk performs that task for determining when to transfer data as described above and therefore allows the processor to communicate with the coprocessor as if the co-processor was directly connected with the processor. Also Since the Kowalczyk interface establishes the network protocol (e.g., see col. 2, lines 41-57) The interface allows the processor to operate independently of the interface requirements of the coprocessor (that would have been connected to the network bus).

14. As to the limitations of claim 24,25 the Gallota taught receiving data via an interface storing data in a memory signaling the coprocessor (or processor) that the data has been stored receiving a read command from the coprocessor (or processor) and providing first data to the coprocessor(or processor) across a boundary wherein the transfer is substantially simultaneous (e.g., see figs. 1,2,3 and col. 2, lines 9-col. 3, line 22).

15. Gallota did not expressly detail (claim 24,25) the signaling was via the first and second interface. However considering the Kowalczyk system the only connecting between buses and therefore connected processors and co-processor would have been via the interfaces (network and DMA interfaces) and therefore the signaling would have been performed in the Gallota and Kowalczyk system via the interfaces (e.g.,see figs. 2,3 of Kowalczyk) . (claims 26-33 are rejected above).

16. It would have been obvious to one of ordinary skill to combine the teachings of Gallota and Kowalczyk. Both references were directed toward control of transfer of data between system devices via a memory with plural input and outputs. Gallota taught the devices to transferring the data were processor and coprocessor that were on different cards or boards. In at least one implementation the transfer of data between the processor memory and coprocessor would have comprises transfer via a system bus. Kowalczyk taught the transfer was between a system bus and a network bus. Clearly the devices in a processing system storing data into a memory for transfer to another device on another bus would have comprised processors. The addition of the control of transfer to be between system bus and network bus would have allowed the combined system to transfer data between processors in a system to co-processors that were connected in a network. This control would have relieved the processor from having to determine when the coprocessor was ready for transfer of data.

Response to Arguments

Applicant's arguments with respect to claims 1-41 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EC

ERIC COLEMAN
PRIMARY EXAMINER